

**IN THE SPECIFICATION**

Page 2, line 1, before "BACKGROUND OF THE INVENTION"  
please insert the following paragraphs:

**--CROSS REFERENCE TO RELATED APPLICATION**

This application claims the benefit and is a continuation  
of U.S. Patent Application No. 09/475,105, filed December 30,  
1999 by Jonathan Douglas et al., now allowed.--

**IN THE CLAIMS**

Please cancel claims 1-36 without prejudice.

Please add new claims 37-42 as follows below.

1           1-36. (Cancelled)

1           37. (New)           A   pipelined instruction decoder for a  
2   multithread processor, the pipelined instruction decoder  
3   comprising:  
4            an instruction decode pipeline to decode  
5   instructions associated with a plurality of instruction  
6   threads, the instruction decode pipeline having a  
7   predetermined number of pipe stages;  
8            a valid bit pipeline in parallel with the  
9   instruction decode pipeline, the valid bit pipeline  
10   having the same predetermined number of pipe stages in  
11   parallel with the predetermined number of pipe stages  
12   of the instruction decode pipeline, the valid bit  
13   pipeline to associate a valid indicator at each pipe  
14   stage with each instruction being decoded in the  
15   instruction decode pipeline; and